What is Claimed is:

1. A method of combining a plurality of signals to form a constant-envelope composite signal for transmission, comprising:

(a) combining a subset of the plurality of signals by majority vote to form a majority voted signal; and

(b) interplex modulating the majority voted signal and others of the plurality of signals to form the constant-envelope composite signal.

2. The method of claim 1, wherein (a) includes:

(a1) determining which of the plurality of signals is in the subset to be majority voted and which of a plurality of interplex modulator inputs receives the majority voted signal as a function of a desired power distribution among the plurality of signals; and

(a2) determining majority voting logic for combining the subset of the plurality of signals as a function of the desired power distribution among the subset of signals.

3. The method of claim 2, wherein (a1) and (a2) are performed when the desired power distribution changes.

4. The method of claim 1, wherein (a) includes combining the subset of signals in accordance with a generalized majority vote scheme.

5. The method of claim 4, wherein the generalized majority vote scheme includes determining a sequence of values of the majority voted signal by interlacing values determined from a majority vote of signals in the subset with values determined from sub-majority votes of less than all of the signals in the subset.

6. The method of claim 5, wherein values of individual signals in the subset are interlaced with values of a majority vote of the signals in the subset.

7. The method of claim 1, wherein the plurality of signals comprises chip-synchronous, pseudo-noise signal codes, and wherein values of the majority voted signal are determined on a chip-by-chip basis.

8. The method of claim 1, wherein each of the plurality of signals is transmitted with a common power efficiency.

9. The method of claim 1, wherein a multiplexing loss resulting from combining the plurality of signals is substantially the same for each of the plurality of signals.

10. The method of claim 1, wherein the plurality of signals includes five signals, and a generalized majority vote is applied to three of the five signals to form the majority voted signal.

11. The method of claim 1, wherein (b) includes:

receiving as interplex input signals the majority voted signal and the others of the plurality of signals;

using the interplex input signals to phase modulate in-phase and quadrature components of a carrier signal;

scaling the in-phase and quadrature components to establish a predetermined power ratio among the interplex input signals; and

combining the in-phase and quadrature components to form the constant-envelope composite signal.

12. The method of claim 11, wherein (b) includes modulating the in-phase and quadrature components via phase shift keying.

13. The method of claim 1, wherein at least some of the plurality of signals contain global positioning information.

14. The method of claim 1, wherein the plurality of signals comprise code division multiple access signals.

15. An apparatus for combining a plurality of signals to form a constant-envelope composite signal for transmission, comprising:

a majority voting logic unit configured to combine a subset of the plurality of signals by majority vote to form a majority voted signal; and

an interplex modulator configured to combine the majority voted signal and others of the plurality of signals to form the constant-envelope composite signal.

16. The apparatus of claim 15, wherein said majority voting logic unit determines which of the plurality of signals is in the subset to be majority voted and which of a plurality of interplex modulator inputs receives the majority voted signal as a function of a desired power distribution among the plurality of signals, said majority voting logic unit further determining majority voting logic for combining the subset of the plurality of signals as a function of the desired power distribution among the subset of signals.

17. The apparatus of claim 16, wherein said majority voting logic unit determines which of the plurality of signals is in the subset to be majority voted, determines which of the plurality of interplex modulator inputs receives the majority voted signal, and determines majority voting logic for combining the subset of the plurality of signals when the desired power distribution changes.

18. The apparatus of claim 15, wherein said majority voting logic unit combines the subset of signals in accordance with a generalized majority vote scheme.

19. The apparatus of claim 18, wherein said majority voting logic unit determines a sequence of values of the majority voted signal by interlacing values determined from a majority vote of signals in the subset with values determined from sub-majority votes of less than all of the signals in the subset.

20. The apparatus of claim 19, wherein said majority voting logic unit interlaces values of individual signals in the subset with values of a majority vote of the signals in the subset.

21. The apparatus of claim 15, wherein the plurality of signals comprises chip-synchronous, pseudo-noise signal codes, and wherein said majority voting logic unit determines values of the majority voted signal on a chip-by-chip basis.

22. The apparatus of claim 15, wherein each of the plurality of signals is represented in the constant-envelope composite signal with a common power efficiency.

23. The apparatus of claim 15, wherein a multiplexing loss resulting from combining the plurality of signals is substantially the same for each of the plurality of signals.

24. The apparatus of claim 15, wherein the plurality of signals includes five signals, and said majority voting logic unit applies a generalized majority vote to three of the five signals to form the majority voted signal.

25. The apparatus of claim 24, wherein said interplex modulator receives three input signals from the majority voting logic unit to be interplex modulated.

26. The apparatus of claim 15, wherein said interplex modulator comprises:

a plurality of phase modulators configured to modulate in-phase and quadrature components of a carrier signal in accordance with interplex input signals received from said majority voting logic unit;

a plurality of attenuators corresponding to the plurality of phase modulators, said attenuators scaling the in-phase and quadrature components to establish a predetermined power ratio among the interplex input signals; and

a signal combiner configured to combine the in-phase and quadrature components to form the constant-envelope composite signal.

27. The apparatus of claim 26, wherein said phase modulators are one of binary phase shift keying modulators and quadrature phase shift keying modulators.

28. The apparatus of claim 15, wherein at least some of the plurality of signals contain global positioning information.

29. The apparatus of claim 15, wherein the plurality of signals comprise code division multiple access signals.

30. The apparatus of claim 15, wherein at least one of said majority voting logic unit and said interplex modulator is remotely programmable.

31. An apparatus for combining a plurality of signals to form a constant-envelope composite signal for transmission, comprising:

means for combining a subset of the plurality of signals by majority vote to form a majority voted signal; and

means for interplex modulating the majority voted signal and others of the plurality of signals to form the constant-envelope composite signal.

32. The apparatus of claim 31, wherein said means for combining includes:

means for determining which of the plurality of signals is in the subset to be majority voted and which of a plurality of interplex modulator inputs receives the majority voted signal as a function of a desired power distribution among the plurality of signals; and

means for determining majority voting logic for combining the subset of the plurality of signals as a function of the desired power distribution among the subset of signals.

33. The apparatus of claim 32, wherein said means for combining determines which of the plurality of signals is in the subset to be majority voted, determines which of the plurality of interplex modulator inputs receives the majority voted signal, and determines majority voting logic for combining the subset of the plurality of signals when the desired power distribution changes.

34. The apparatus of claim 31, wherein said means for combining combines the subset of signals in accordance with a generalized majority vote scheme.

35. The apparatus of claim 34, wherein said means for combining determines a sequence of values of the majority voted signal by interlacing values determined from a majority vote of signals in the subset with values determined from sub-majority votes of less than all of the signals in the subset.

36. The apparatus of claim 35, wherein said means for combining interlaces values of individual signals in the subset with values of a majority vote of the signals in the subset.

37. The apparatus of claim 31, wherein the plurality of signals comprises chip-synchronous, pseudo-noise signal codes, and wherein said means for combining determines values of the majority voted signal on a chip-by-chip basis.

38. The apparatus of claim 31, wherein each of the plurality of signals is represented in the constant-envelope composite signal with a common power efficiency.

39. The apparatus of claim 31, wherein a multiplexing loss resulting from combining the plurality of signals is substantially the same for each of the plurality of signals.

40. The apparatus of claim 15, wherein the plurality of signals includes five signals, and said means for combining applies a generalized majority vote to three of the five signals to form the majority voted signal.

41. The apparatus of claim 40, wherein said means for interplex modulating receives three interplex input signals from the means for combining.

42. The apparatus of claim 31, wherein said means for interplex modulating comprises:

means for phase modulating in-phase and quadrature components of a carrier signal in accordance with interplex input signals received from said means for combining;

means for attenuating the in-phase and quadrature components to establish a predetermined power ratio among the interplex input signals; and

means for combining the in-phase and quadrature components to form the constant envelope composite signal.

43. The apparatus of claim 42, wherein said means for phase modulating is one of binary phase shift keying modulators and quadrature phase shift keying modulators.

44. The apparatus of claim 31, wherein at least some of the plurality of signals contain global positioning information.

45. The apparatus of claim 31, wherein the plurality of signals comprise code division multiple access signals.